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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,808	08/28/2003	Klaas Bult	1875.0510002	5778
26111	7590	03/01/2004	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			LAM, TUAN THIEU	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/649,808	Applicant(s) BULT ET AL.	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/28/2003</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 1, line 2, the US application no. 10/083,463 is now USP 6,639,430. Page 27, line of paragraph [0093], "308" and "310" is supposed to be --306 and --308--, respectively. Correction is required.

Appropriate correction is required.

Drawings

2. Figures 2A, 2B and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-12 and 15-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 7, the recitation of "capable of" in lines 3 and 4 is indefinite because it is not a positive recitation. It is suggested to change "capable of" to --for--.

In claims 4 and 10, the recitation of "capable of" in line 1 is indefinite because it is not a positive recitation. It is suggested to change "capable of" to --for--.

In claim 15, the recitation of "capable of" in lines 2 and 3 is indefinite because it is not a

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positive recitation. It is suggested to change “capable of” to --for--.

Claims 2-3, 5-6, 8-9, 11-12 and 16 are indefinite because of the technical deficiencies of claims 1, 7 and 15.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pelley, III (USP 4,551,641). Figure 1 of Pelley shows a reset circuit (22, 23, 25, 28, 29) for a latch circuit (26, 27) having bistable pair of transistors connected to a supply voltage (Vcc, ground), the reset circuit comprising a first transistor (22 or 23) connected to the supply voltage, a second transistor (28) connected between said first transistor and a first port (36), a third transistor connected between said first transistor and a second port (35) as called for in claims 13-14.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuya (USP 6,191,624). Figure 1 of Matsuya shows a comparator comprising analog input signal (Vin), a reference signal (Vref), digital output signal (Vout), said comparator comprising a latch circuit having a bistable pair of transistors (T12, T22) coupled between a reset circuit (125, 126) and a first supply voltage (Vdd), and a vertical latch (123, 124) coupled between said first supply

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voltage and a second supply voltage (ground) and coupled to said bistable pair of transistors, said vertical latch having first transistor (T2) and second transistor (T3) as called for in claims 15-16.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-7 and 17-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5, 8, 11 of U.S. Patent No. 6,639,430. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the present invention is anticipated by the claim 1 of the USP 6,639,430. Claim 1 of the USP 6,639,430 recites a bistable pair of transistors connected between a reset switch and said first supply voltage, and having a first port capable of receiving a first current signal and producing a first output voltage, and a second port capable of receiving a second current signal and producing a second output voltage, and a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port, said vertical latch having a transistor (fourth transistor) connected said first supply voltage but

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isolated from said second supply (third transistor causes the fourth transistor being isolated from the first supply voltage).

Regarding claim 2 of the present invention, claim 5 of USP 6,639,430 recited the first transistor is MOSFET.

Regarding claim 3 of the present invention, claim 3 of USP 6,639,430 recites reset switch is microelectronmechanical reset switch (MOSFET).

Regarding claim 4 of the present invention, claim 2 of USP 6,639,430 recites said vertical latch is capable of decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.

Regarding claim 5 of the present invention, claim 8 of USP 6,639,430 recites a vertical latch reset switch connected to said vertical latch.

Regarding claim 6 of the present invention, claim 11 of USP 6,639,430 recites a second vertical latch connected between said first supply voltage and said second supply voltage, and connected to said second port (bistable pair of transistors).

Regarding claim 7 of the present invention, claim 4 of USP 6,639,430 recites a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port capable of receiving a first current signal and producing a first output voltage, and a second port capable of receiving a second current signal and producing a second output voltage, and a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port, wherein said vertical latch comprising a first current mirror pair connected to said bistable pair of transistors, a second current mirror pair connected to said first current mirror pair.

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Regarding claim 17 of the present invention, claim 25 of USP 6,639,430 recites method for decreasing the time in a latch circuit port receiving a current signal greater than a bias current reaches a steady state voltage, comprising the steps of amplifying the current signal greater than the bias current while maintaining a current signal less than the bias current received at a second latch circuit port, and applying said amplified current signal to the latch circuit port receiving the current signal greater than the bias current.

Regarding claim 18 of the present invention, claim 26 of USP 6,639,430 recites the steps of resetting the bistable pair and the vertical latch, and holding the fourth transistor OFF during said resetting.

Regarding claim 19 of the present invention, claim 27 of USP 6,639,430 recites the steps of holding the third transistor OFF during said resetting.

Regarding claim 20 of the present invention, claim 28 of USP 6,639, 430 recites after said resetting, holding the fourth transistor OFF when the second transistor changes states from ON to OFF.

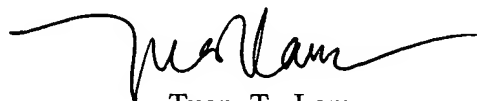
Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's cited prior art has been considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam
Primary Examiner
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2/10/2004